

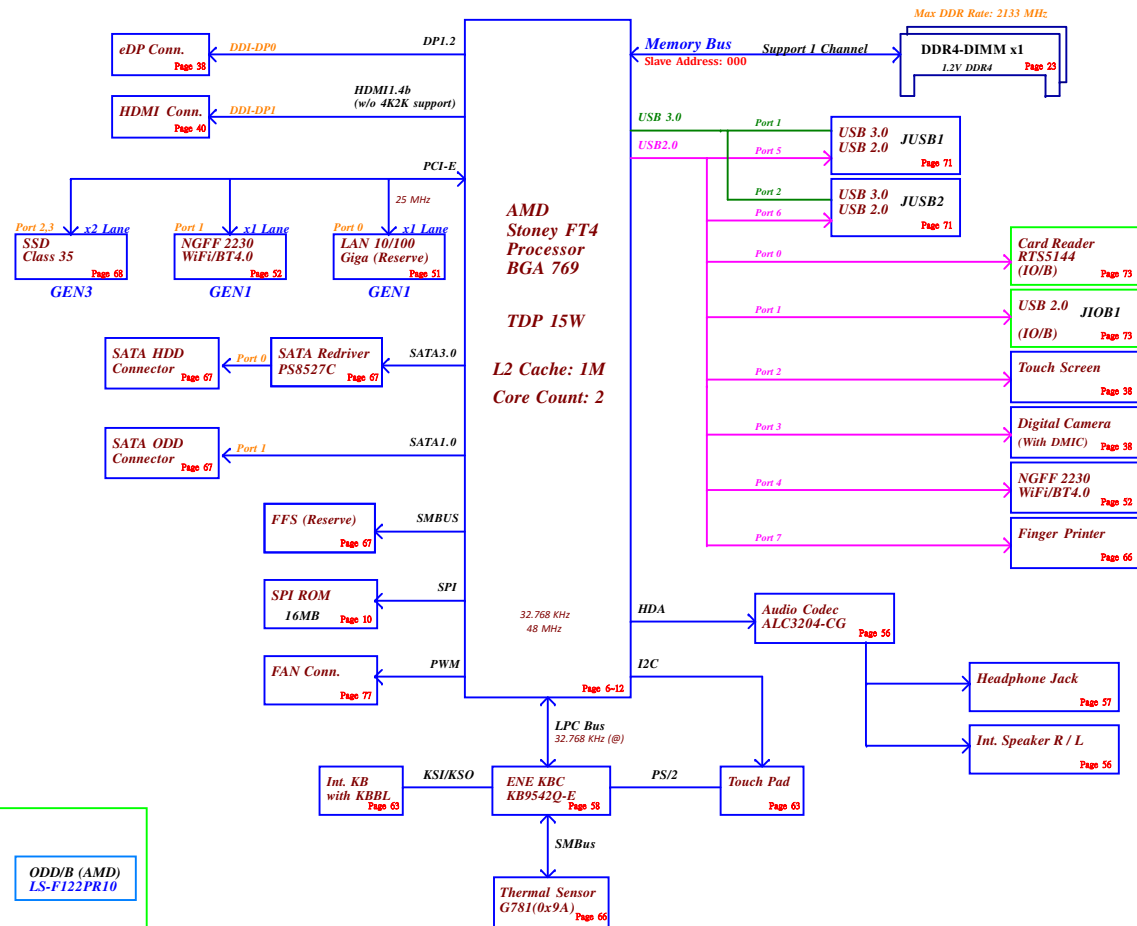
Dell / Compal Confidential

Schematic Document

AMD Stoney Ridge

2018-05-21 Rev: 1.0 (A00)

## SUB-BOARDS



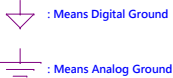
Board ID Table for AD Channel:

Vcc	3.3V +/- 1%				
Ra(RE5)	100K +/- 1%				
Board ID	Rb(RE9)	VAD min	VAD typ	VAD max	EC AD3
0	0 ohm	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table:

Board ID	Definition
0	N3V3 MLK STR UMA <EVT>
1	N3V3 MLK STR UMA <DVT1>
2	N3V3 MLK STR UMA <DVT2>
3	N3V3 MLK STR UMA <PVT>
4	N/A
5	N/A
6	N/A
7	N/A
8	N/A
9	N/A
10	N/A
11	N/A
12	N/A
13	N/A
14	N/A
15	N/A
16	N/A
17	N/A
18	N/A
19	N/A

Symbol Note :



SMBUS Control Table:

	SOURCE	BATT	Charger	Thermal Sensor	Touch Pad	DIMM	FFS
EC_SMB_CR1 EC_SMB_DA1	KB9542Q	V	V				
EC_SMB_CR2 EC_SMB_DA2	KB9542Q			V			
TP_CLK TP_DATA	KB9542Q				V		
APU_SCLK0 APU_SDATA0	APU					V	V
APU_SIC APU_SID	APU			V			

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+5VALW	System +5VALW power rail	ON	ON	ON*
+3VALW	System +3VALW power rail	ON	ON	ON*
+1.8V_ALW	System +1.8VALW power rail	ON	ON	ON*
+0.95VALW	System +0.95VALW power rail	ON	ON	ON*
+0.775VALW	System +0.775VALW power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR4 +0.6V power rail	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+0.95VS	System +0.95VS power rail	ON	OFF	OFF
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Core NB voltage for APU	ON	OFF	OFF
+VDDCR_FCH_ALW	S5 supply voltage for the FCH core logic	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON
+0.95VS_APU_GFX	PCIe GPP, PCIe GFX, DP and SATA PHY logic power rail for APU	ON	OFF	OFF
+3VS_APU	+3VS power rail for APU	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF				

HS I/O	USB3.0	
	Port 0	---
	Port 1	USB3 Connector Port 1
	Port 2	USB3 Connector Port 2
	USB2.0	
	Port 0	Card Reader (IO/B)
	Port 1	USB2 Connector Port (IO/B)
	Port 2	Touch Screen
	Port 3	Camera
	Port 4	WLAN
	Port 5	USB2 Connector Port 1
	Port 6	USB2 Connector Port 2
	Port 7	Finger Printer
	SATA	
	Port 0	HDD
	Port 1	ODD
	Display(DP)	
	Port 0	eDP (Lan0/Lan1)
	Port 1	HDMI (Lan0/Lan1/Lan2/Lan3)
	Port 2	---

Clock Signal		
GFX_CLK	---	
GPP_CLK0	LAN	
GPP_CLK1	WLAN	
GPP_CLK2	NVMe SSD	
GPP_CLK3	---	
PCI Express(GFX)		
Lane 0	---	
Lane 1	---	
Lane 2	---	
Lane 3	---	
PCI Express(GPP)		
Lane 0	LAN	
Lane 1	WLAN	
Lane 2	NVMe SSD	
Lane 3	NVMe SSD	

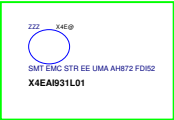


## 2019/4/26



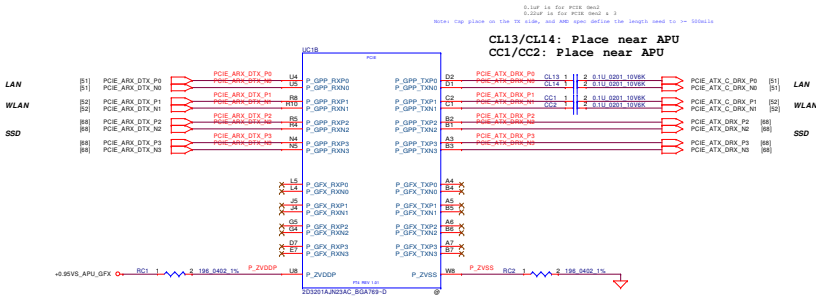
Security Classification	Compul Secret Data		15a <b>Compul Electronics, Inc.</b> <b>Power Section Diagram</b> Docu. Number <b>LA-872P</b> Date: 12/28/87 09:58:18 Printed: 5 of 102
Issued Date	2016/01/07	Declassified Date	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE AIR FORCE WITHOUT PERMISSION AS AUTHORIZED BY COMPAUL ELECTRONICS, INC. THIS SHEET AND THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT WRITTEN CONSENT OF COMPAUL ELECTRONICS, INC.			
			Rev. 1 (4/00)

EMC X4E for BOM control:

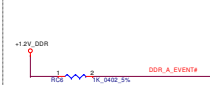


2015/02/12, Change to 2 Mark P/N

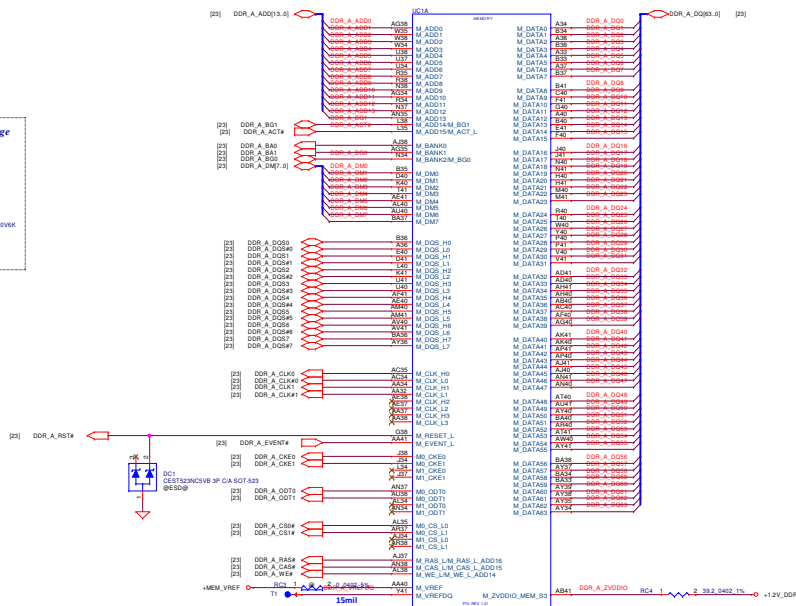
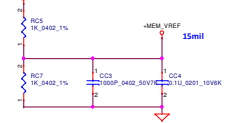
15W APU R1 P/N	15W APU R3 P/N
UC1 NPI used D Mark P/N SA000807LL A4 J108 S IC A8-9225 AM925AYN23AC 2.6G APU S	UC1 SA000807LL A4 J108 S IC A8-9225 AM925AYN23AC 2.6G APU A311
UC1 NPI used D Mark P/N SA000808LL A4 J108 S IC A8-9425 AM9425AYN23AC 3.1G APU S	UC1 SA000808LL A4 J108 S IC A8-9425 AM9425AYN23AC 3.1G APU A311



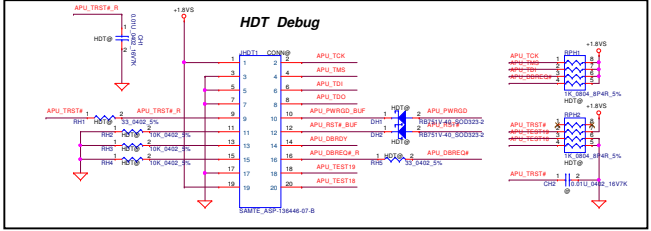
EVENT# pull high



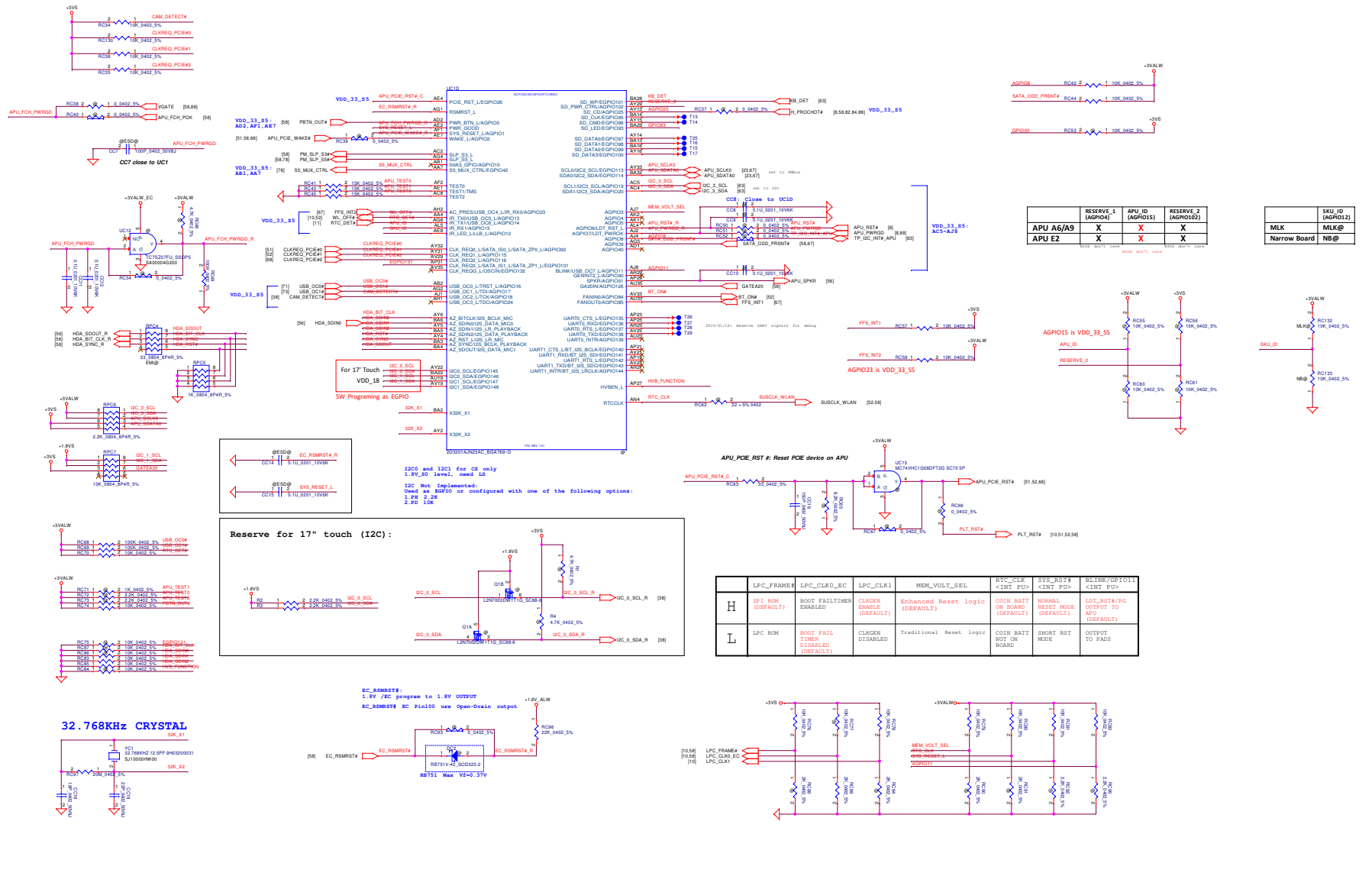
+1.2V\_DDR



Place them close to APU within 1"







	RESERVE_1 (AGPIO4)	APU_ID (AGPIO15)	RESERVE_2 (AGPIO102)
APU A6/A9	X	X	X
APU E2	X	X	X

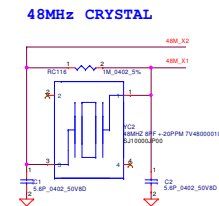
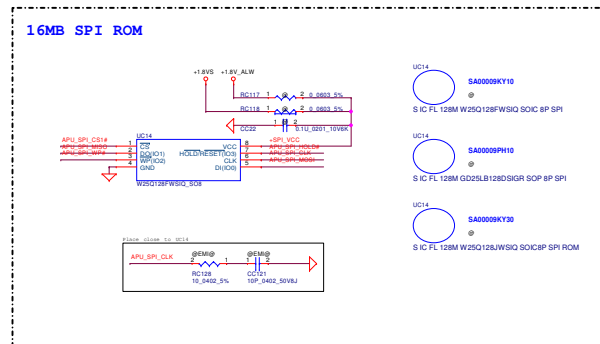
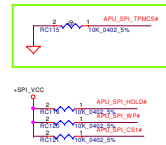
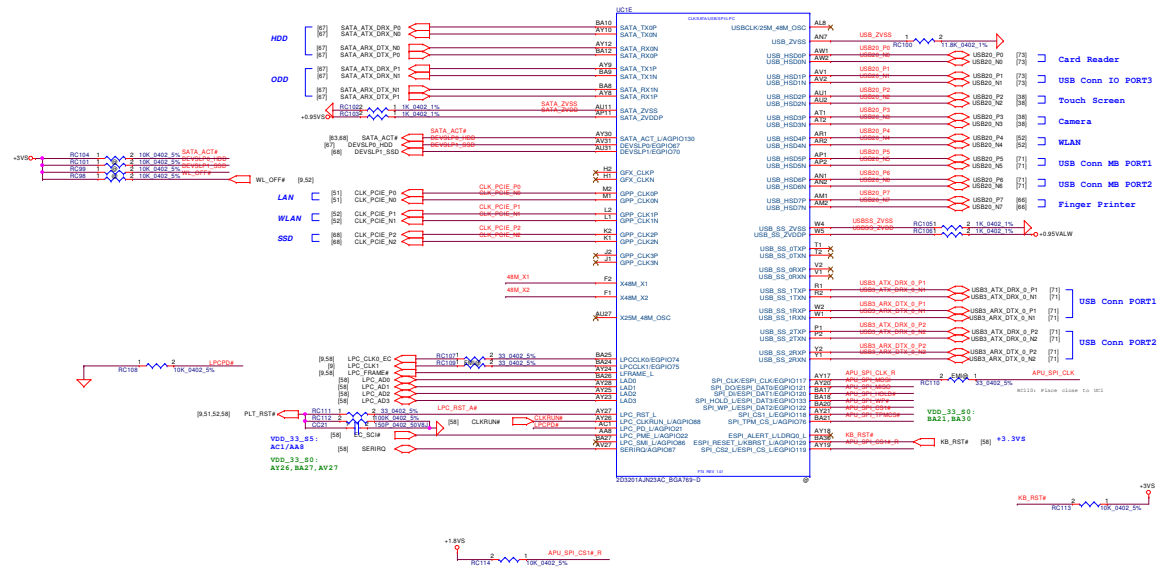
	SKU ID (AGPIO12)
MLK	MLK@
Narrow Board	NB@

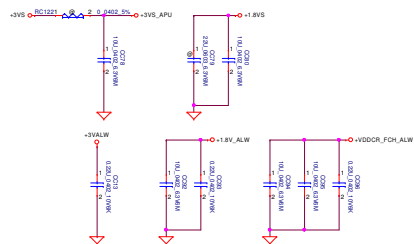
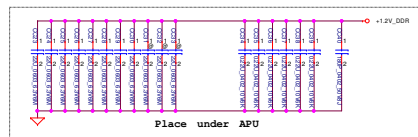
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	MEM_VOLT_SEL	RTC_CLK LPC_FU#	SYS_RST# LPC_FU#	BLINK/OTP10# LPC_FU#
H	SPT ROM (DEFAULT)	BOOT FAILTIMER ENABLED	CLGEN ENABLED (DEFAULT)	Enhanced Reset logic (DEFAULT)	COIN BATT ON BOARD (DEFAULT)	NORMAL RESET MODE (DEFAULT)	INT_RST#/PG OUTPUT TO INT# (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER (DEFAULT)	CLGEN DISABLED	Traditional Reset logic (DEFAULT)	COIN BATT NOT ON BOARD	SHORT RST MODE	OUTPUT TO PADS

(#55350 ) AGPIO Power Domain:

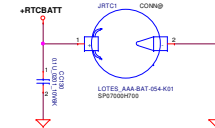
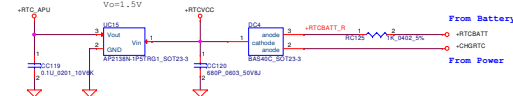
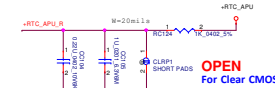
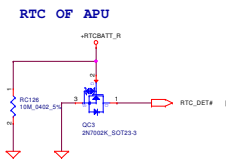
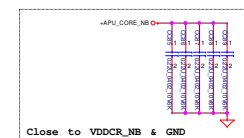
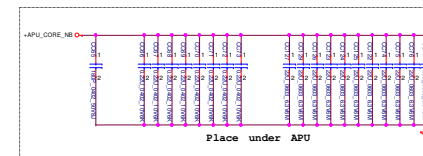
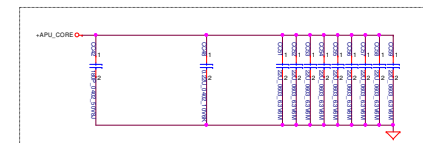
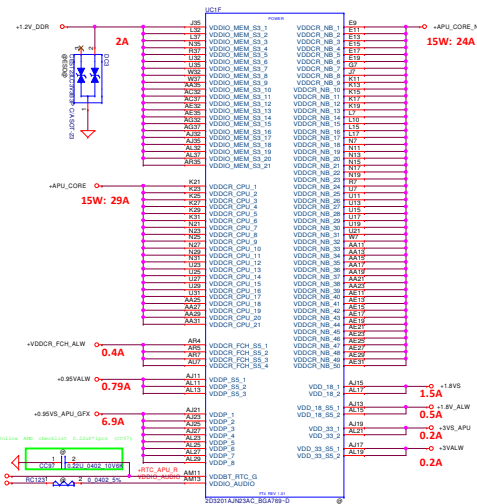
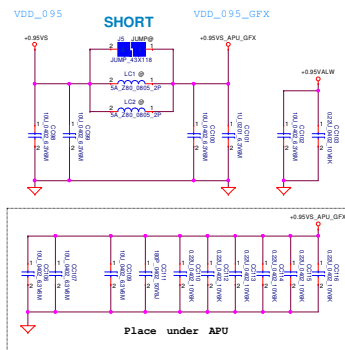
VDD\_3.3\_S5: Connect to +3VALW

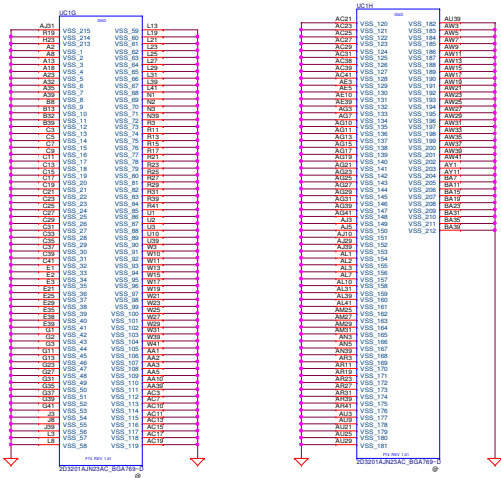
VDD\_3.3\_S0: Connect to +3VS

[illegible]



+0.95VS OF APU





# Reserve

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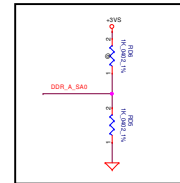
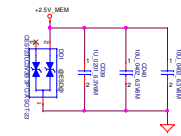
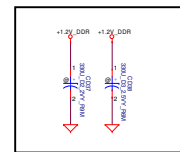
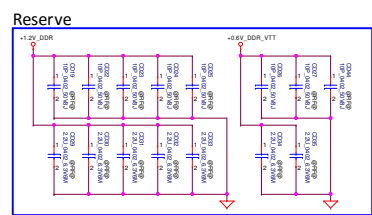
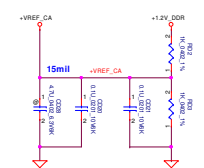
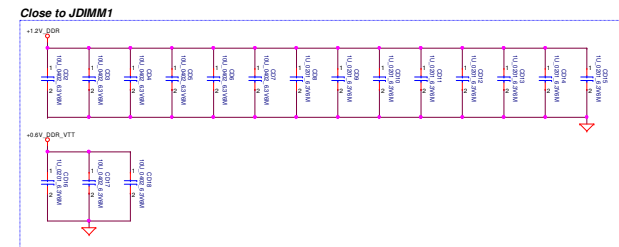
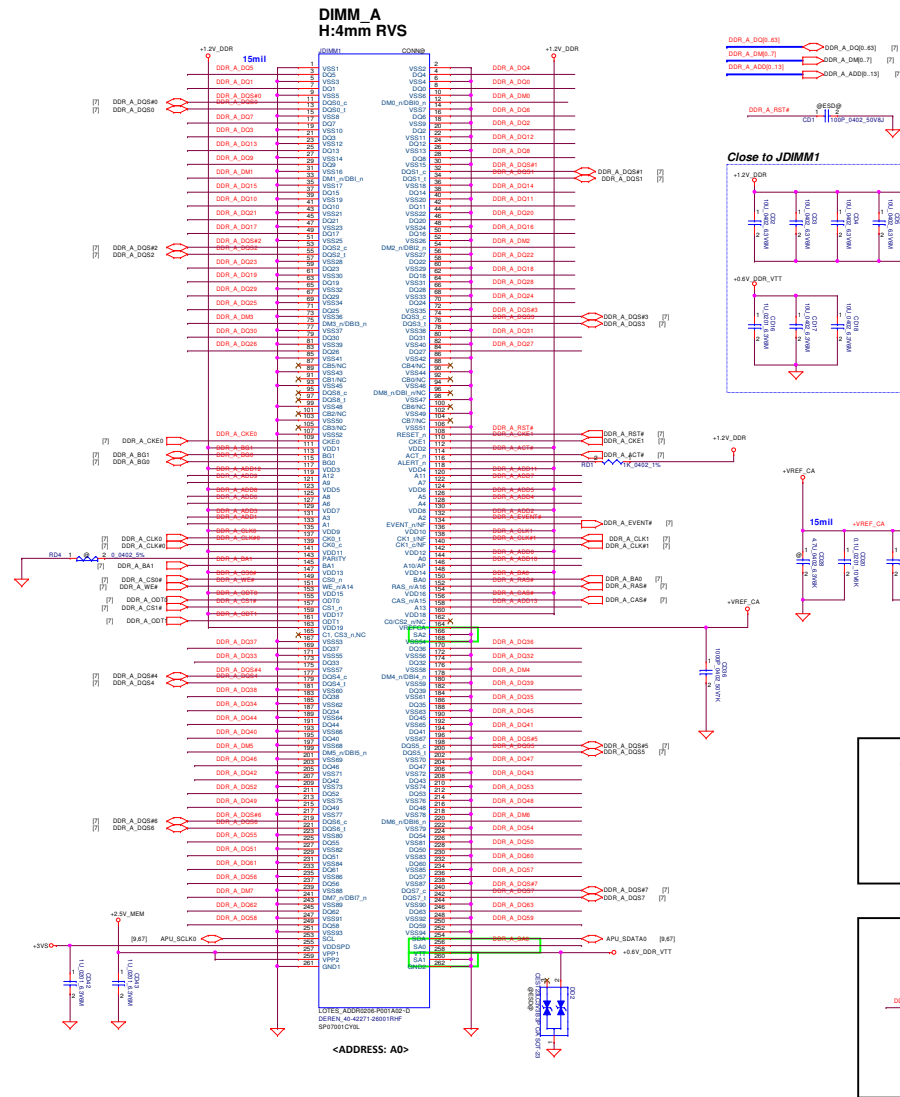
# Reserve

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2019/03/15:  
Due to CLK connect to Port0 & Port1 (Page.7)  
Reference the CRB design, need to follow DIMM400 setting :  
Slave Address as 000 (SA0/SA1/SA2)

# Reserve



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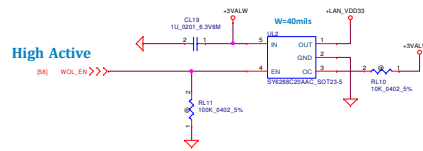
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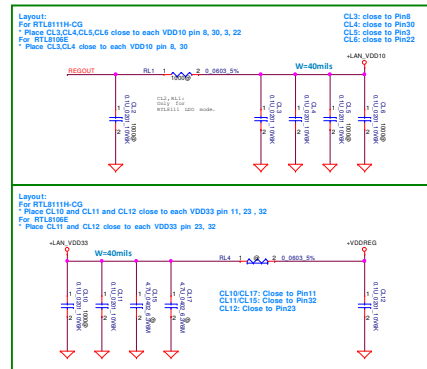
# Reserve

# Reserve

+LAN\_VDD33 Rising time (10%~90%)  
Need to: >0.5mS & <100mS.



	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CG2 (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

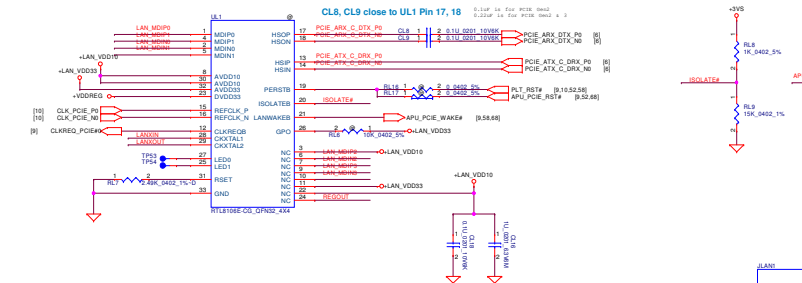
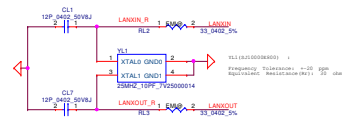


## LAN CHIP 10/100/1000

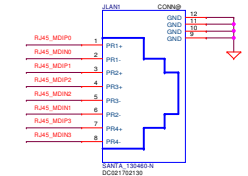
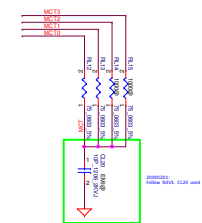
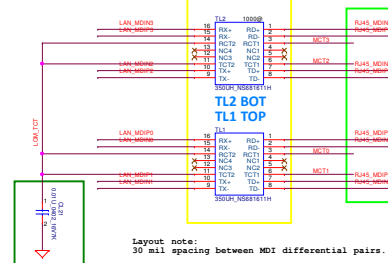
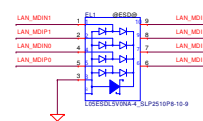
RTL8111H-CG	RTL8111G-CG2
RTL8106E-CG	RTL8106G-CG2
LDO mode	LDO mode
10/100M	10/100/1000M



Note: Giga LAN (Reserve)



## LAN Transformer 10/100M x2



Layout note:  
30 mil spacing between MDI differential pairs.

Main:  
SP050009800, 5 XFORM, NS681611H LAN  
2nd:  
SP050006W00, 5 XFORM, HD-245 10/100 PC CARD LAN

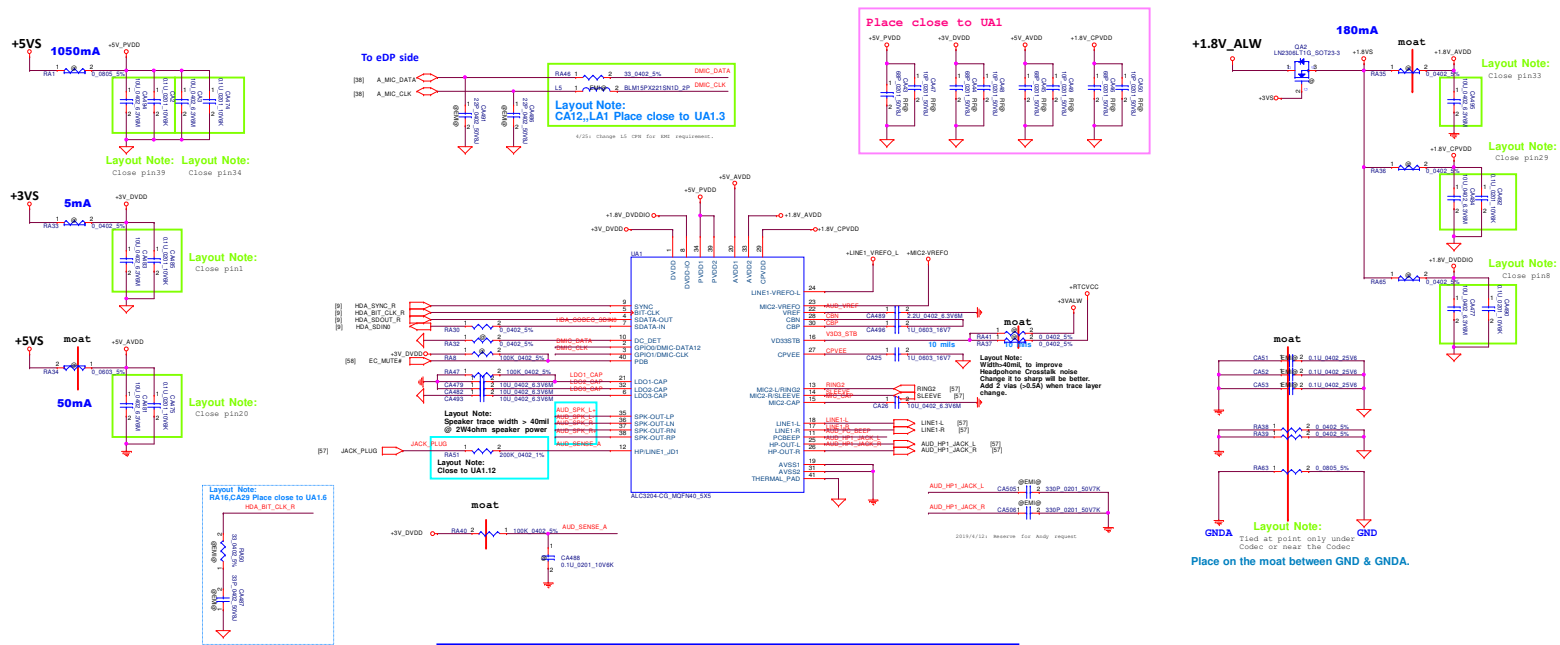


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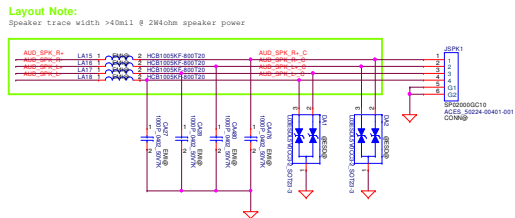
# Reserve

# Reserve

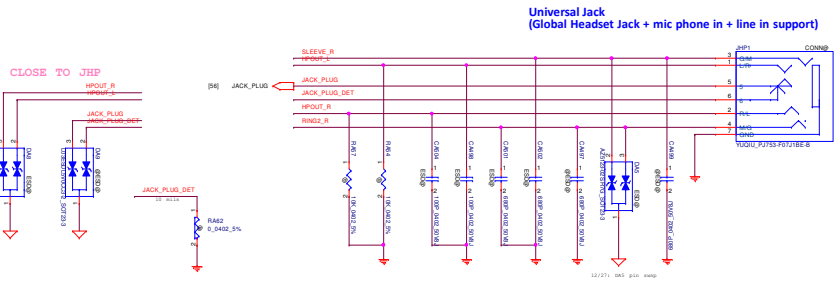
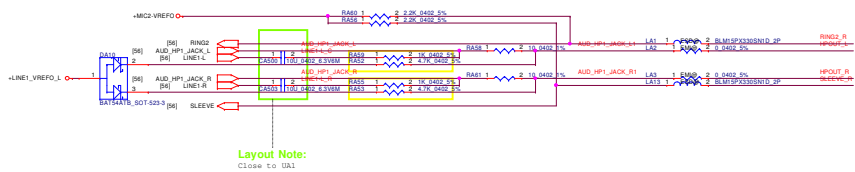
Main Func = Audio



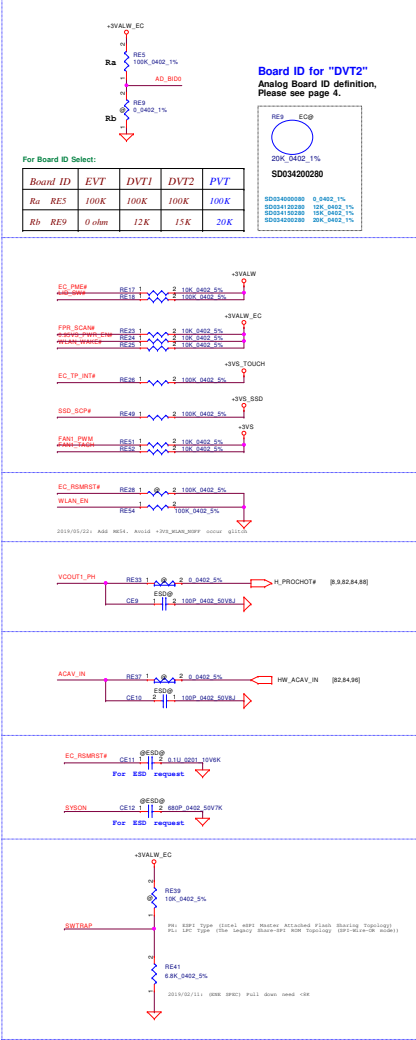
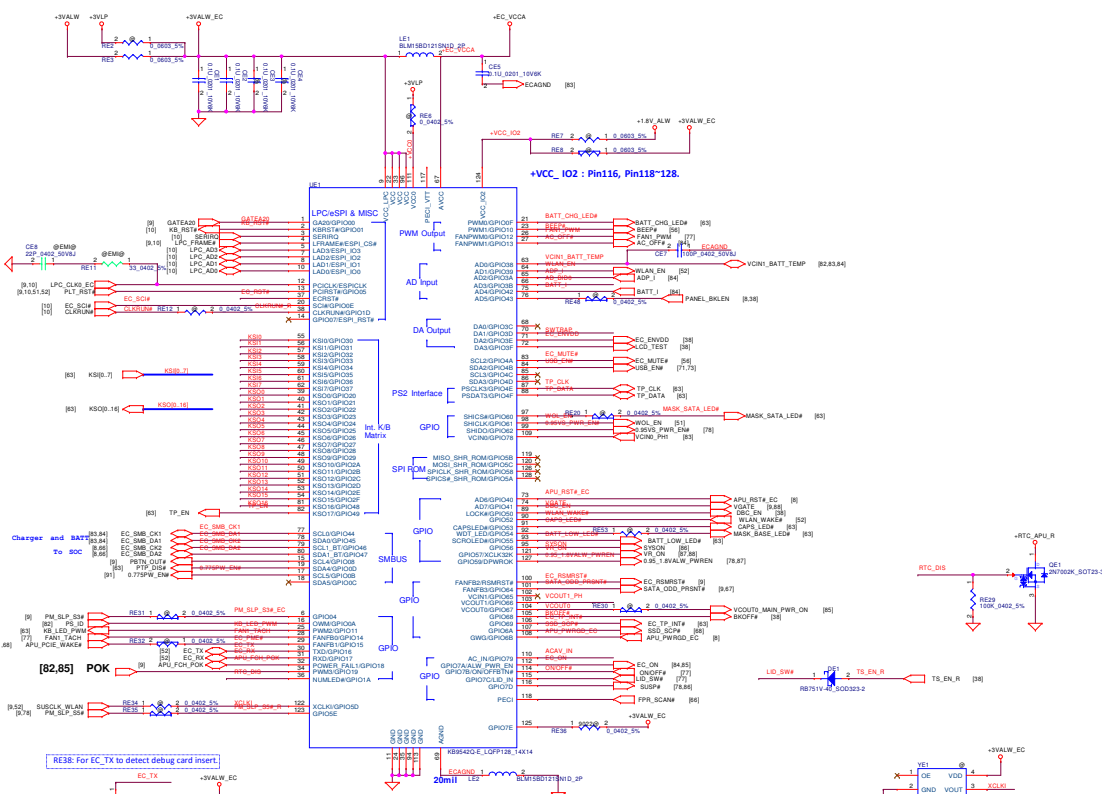
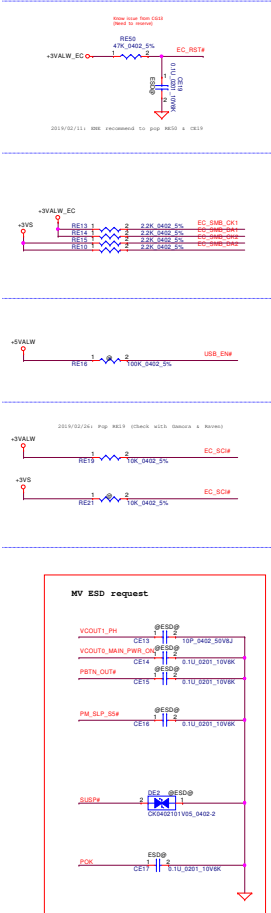
Main Func = Speaker







2019/03/21:  
Change UE1 from B to E version.



# Reserve

# Reserve

**2019/01/21: Finished.**

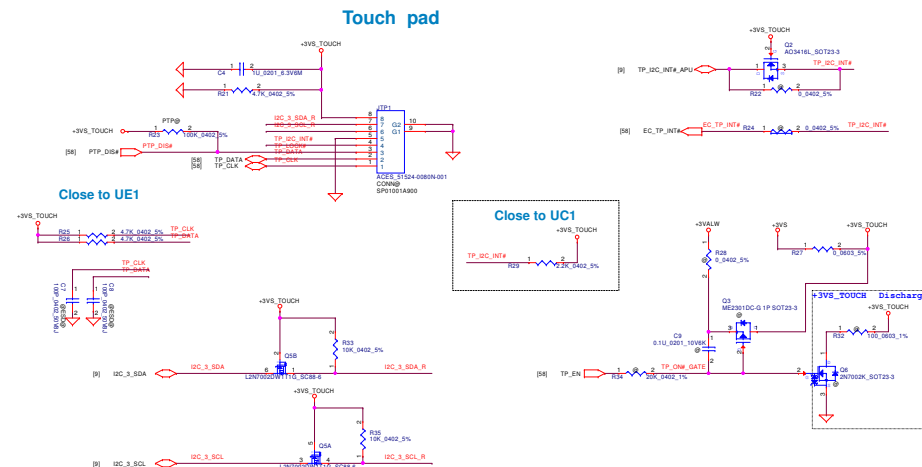


**KBC**  
**KB9542Q-E**

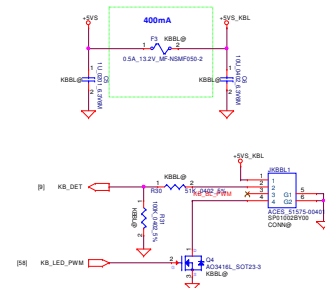
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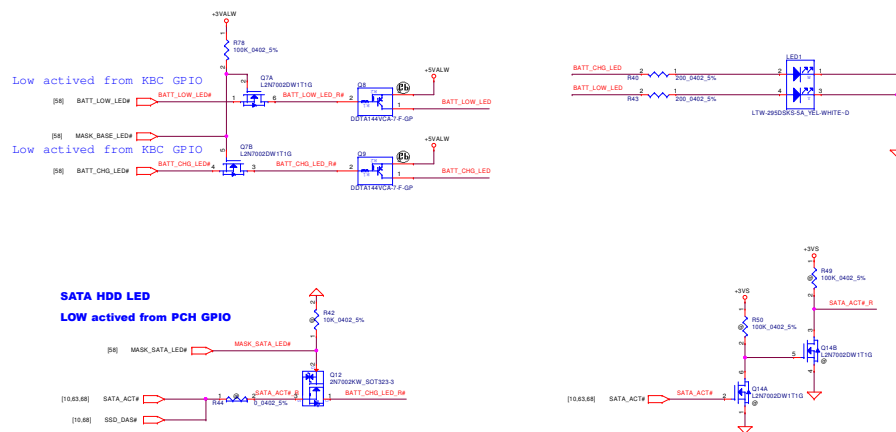
**Main Func = Touch Pad**



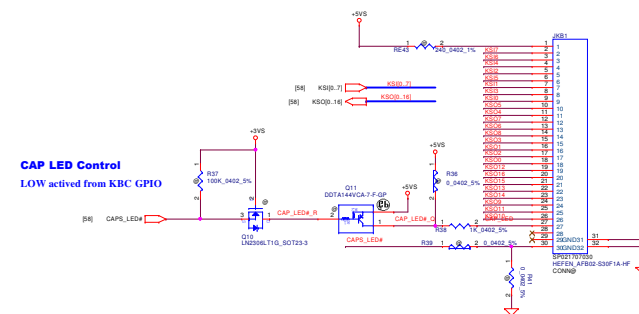
## Main Func = KBBI




Main Func = LED



Main Func = KB



Security Classification	Compul Secret Data			
Issued Date	2016/01/07	Deciphered Date	2017/01/07	Title <b>TP / KB / KBBL / LED</b>
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01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100			01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100	

# Reserve

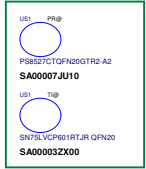
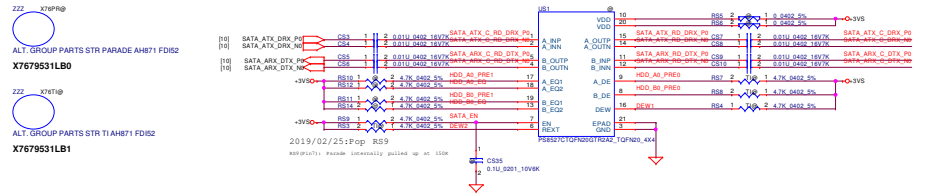


# Reserve



Main Func = HDD

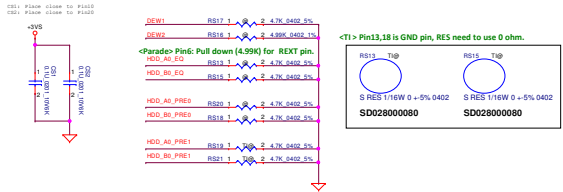
SATA X76 for BOM control:



2019/02/25: Update SATA re-driver strap table

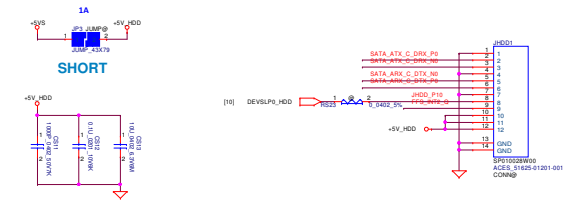
Pull High											
PIN	PIN 6	PIN 8	PIN 9	PIN 13	PIN 16	PIN 17	PIN 18	PIN 19		PIN 10	PIN 20
TI	DEW2	DE2	DE1	GND	DEW1	EQ1	GND	EQ2		VCC	VCC
Parade	RXS7	B_DE	A_DE	B_EQ2	DEW	A_EQ1	A_EQ2	B_EQ1		RXS5	RXS6
Location	RS3	RS8	V7	RS14	RS4	RS10	RS12	RS11		V	V
TI	V	V	V	NC	V	NC	NC	NC		V	NC
Parade	NC	NC	NC	NC	NC	NC	NC	NC		V	V

Pull Down											
PIN	PIN 6	PIN 8	PIN 9	PIN 13	PIN 16	PIN 17	PIN 18	PIN 19		PIN 7	
TI	DEW2	DE2	DE1	GND	DEW1	EQ1	A_EQ2	B_EQ2		EN	
Parade	RXS7	B_DE	A_DE	B_EQ2	DEW	A_EQ1	A_EQ2	B_EQ1		EN	
Location	RS16	RS18	RS20	RS15	RS17	RS19	RS13	RS21		RS9	
TI	NC	NC	NC	V	NC	V	V	V		V	
Parade	NC	NC	NC	NC	NC	NC	NC	NC		V	



2019/02/25: Change RS19,RS21 BOM structure to TI@

+5V\_HDD Source



8.3.2 Output De-Emphasis

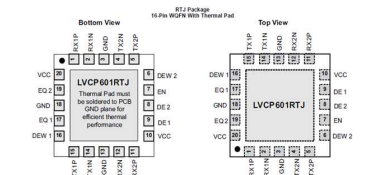
The SN76LVCP601 device provides the de-emphasis settings shown in Table 1. De-emphasis control is independent for each channel, controlled by the DE1 and DE2 pin settings as shown in Table 1. The reference for the de-emphasis settings available in the device is the transition bit amplitude for each given configuration; this transition bit amplitude is different at 0 dB than the -2-dB and -4-dB settings by design. DEW1 and DEW2 control the DE durations for channels one and two, respectively. Table 1 lists the recommended settings for these control pins. Output de-emphasis is capable of supporting FRM trace at the output anywhere from 2 in. (5.1 cm) to 12 in. (30.5 cm) at SATA 3G/6G speed.

Table 1. TX and RX EQ and DE Pulse-Duration Settings

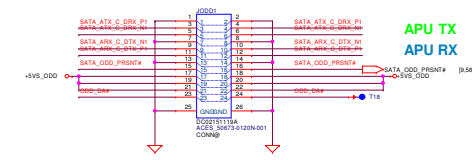
DE1 OR DE2		CH1 OR CH2 DE EMPHASIS (dB at 6 Gbps)	EQ1 OR EQ2	CH1 OR CH2 Equalization (dB at 6 Gbps)	PL RS19 / RS21 PH RS10 / RS11
NC (default)	0	-4	NC (default)	0	
0	0	-2	0	7	
1	1	-2	1	14	
DEW1 OR DEW2	DEW1 OR DEW2	DEVICE FUNCTION -- DE WIDTH FOR CH1/CH2			
0	0	De-emphasis pulse duration, short			
1 (default)	1 (default)	De-emphasis pulse duration, long			

SN76LVCP601  
SATA 3G/6G SERDES WITH 10-PIN WQFN WITH THERMAL PAD

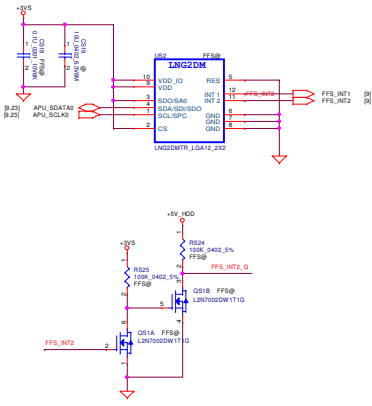
5 Pin Configuration and Functions



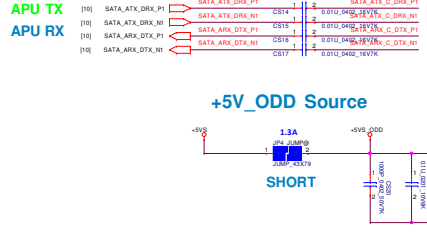
SATA ODD Connector (FFC Type)

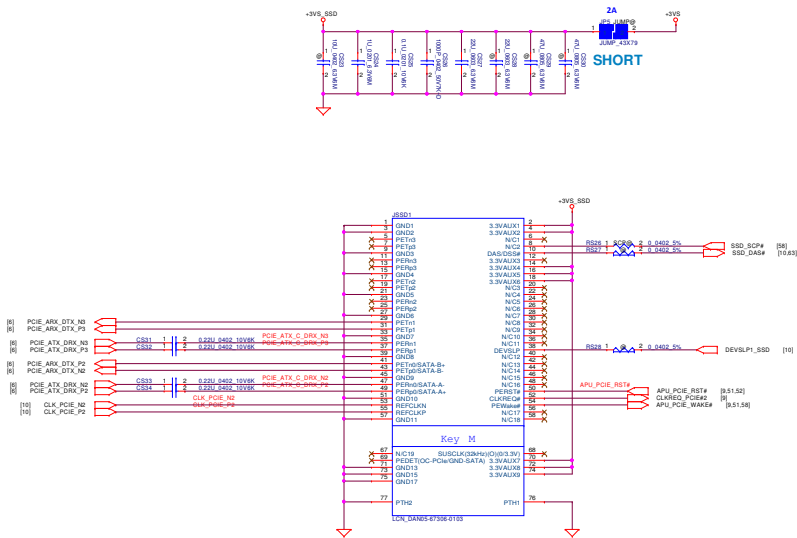


Main Func = FFS



Main Func = ODD

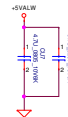




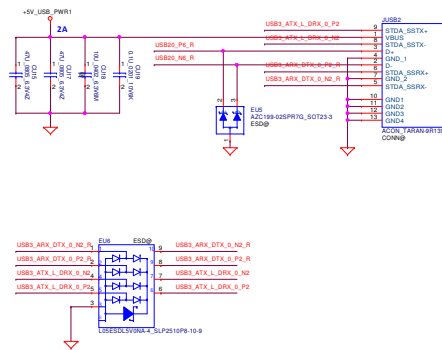
# Reserve

# Reserve

## 12/25: Fla Sweep LU1, LU2, LU3, LU4, LU5



10. *Journal of the American Medical Association*, 2000; 284: 2689-2694.



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			Document Number	
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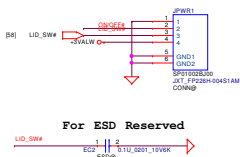
# Reserve

# Reserve

# Reserve

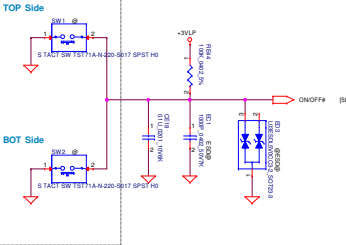
Main Func = POWER BTN

Power button



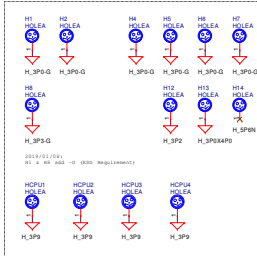
Pop only before MP

ON/OFF switch

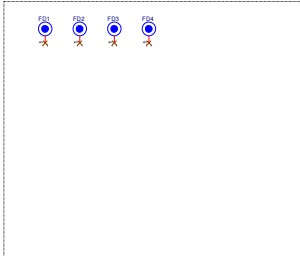


Main Func = Screw Hole

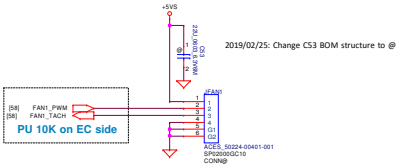
Screw Hole



FD



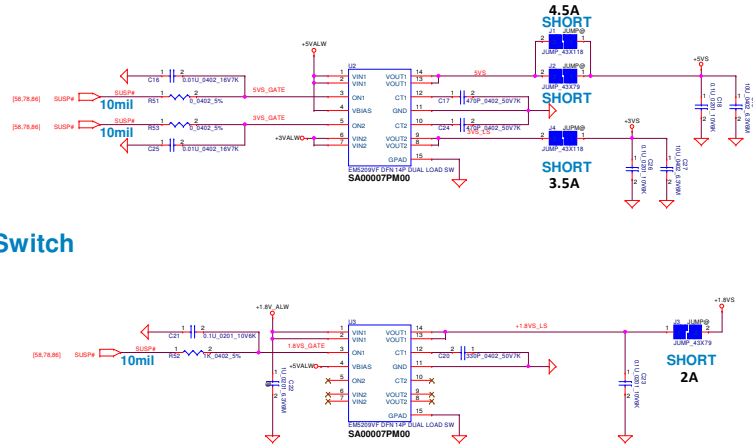
Main Func = FAN Control



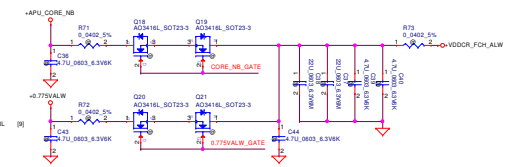
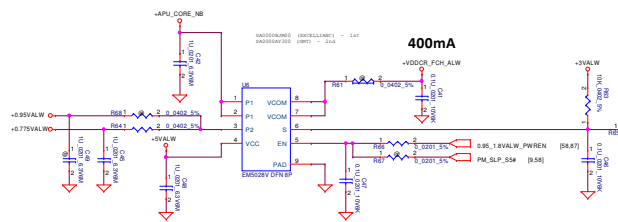
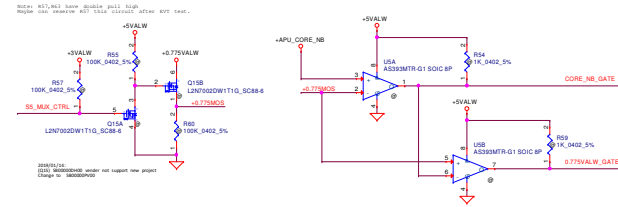
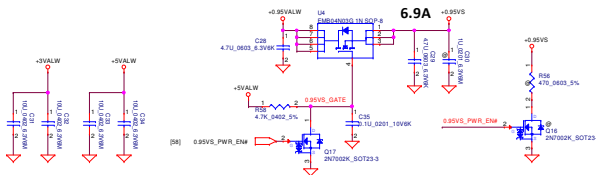
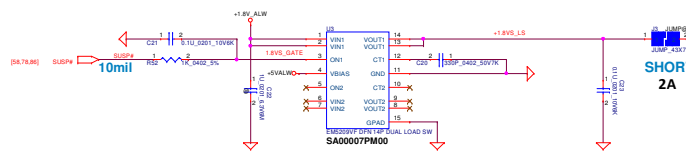
Main Func = PCB P/N

Part Number	Description
DA60026R000	PCB 20F LA-H872P REV0 M/B 3
DA60026R000	PCB 20F LA-H872P REV0 M/B 3
DA60026R000	PCB 20F LA-H872P REV0 M/B 3
DA60026R000	PCB 20F LA-H872P REV0 M/B 3

+5VS and +3VS Switch



+1.8VS Switch




# Reserve

# Reserve

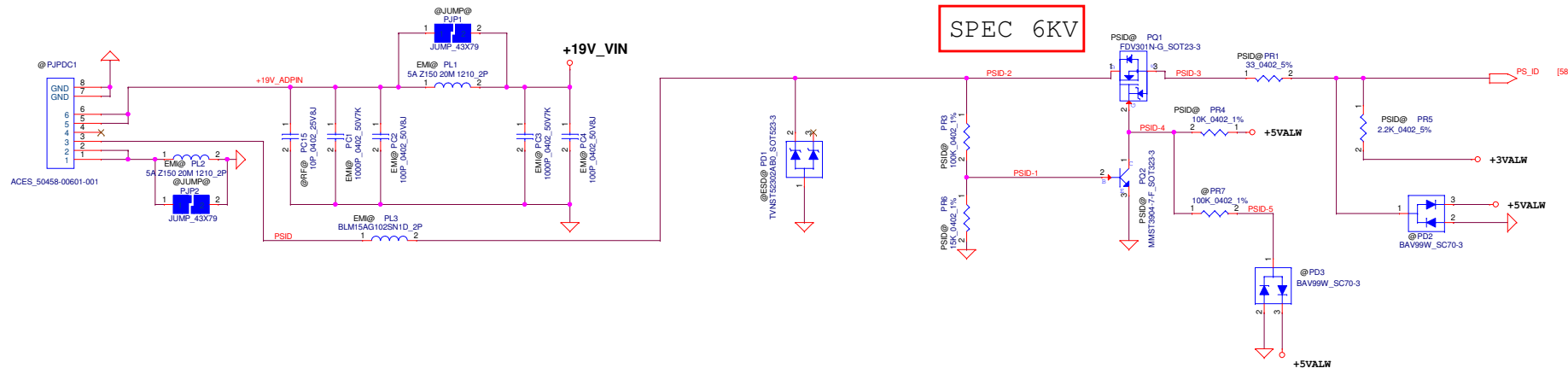


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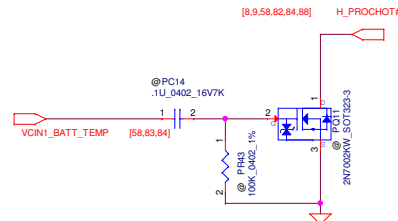
		
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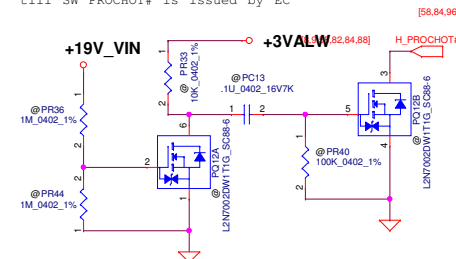
#### Adapter protection

if battery removed, adaptor only,  
then trigger the H\_PROCHOT#,  
keep @ in BOM since battery can not  
be removed by end user

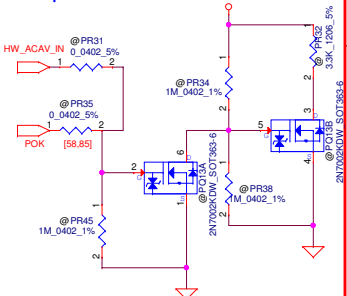


#### Battery protection

asserts H\_PROCHOT# when adaptor is  
unplugged, keep low for 10ms  
till SW PROCHOT# is issued by EC



#### Erp lot6 Circuit



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PWR\_DCIN/BATT CONN/IOTP

LA-H872P

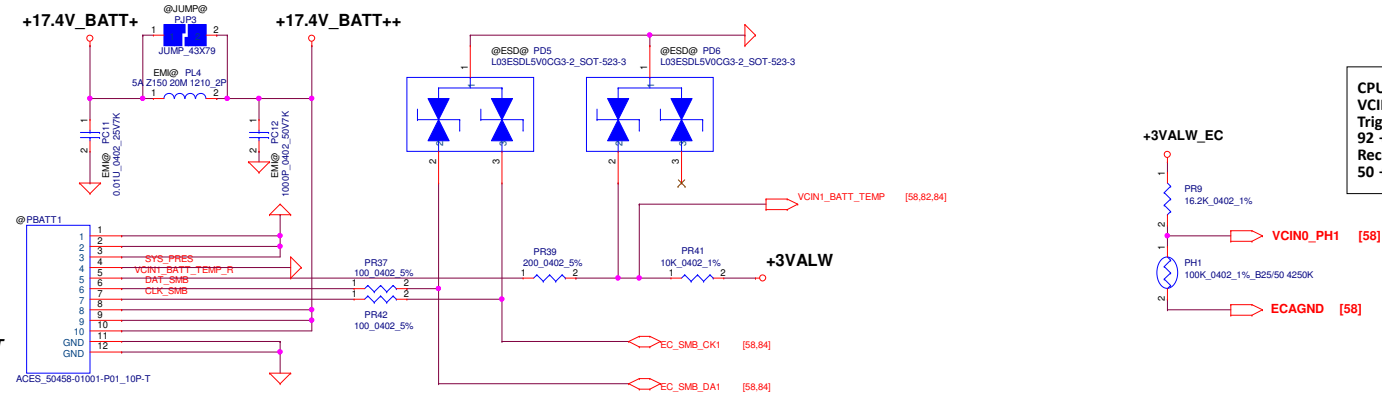
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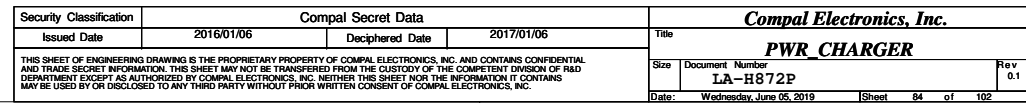
Battery Bot Side

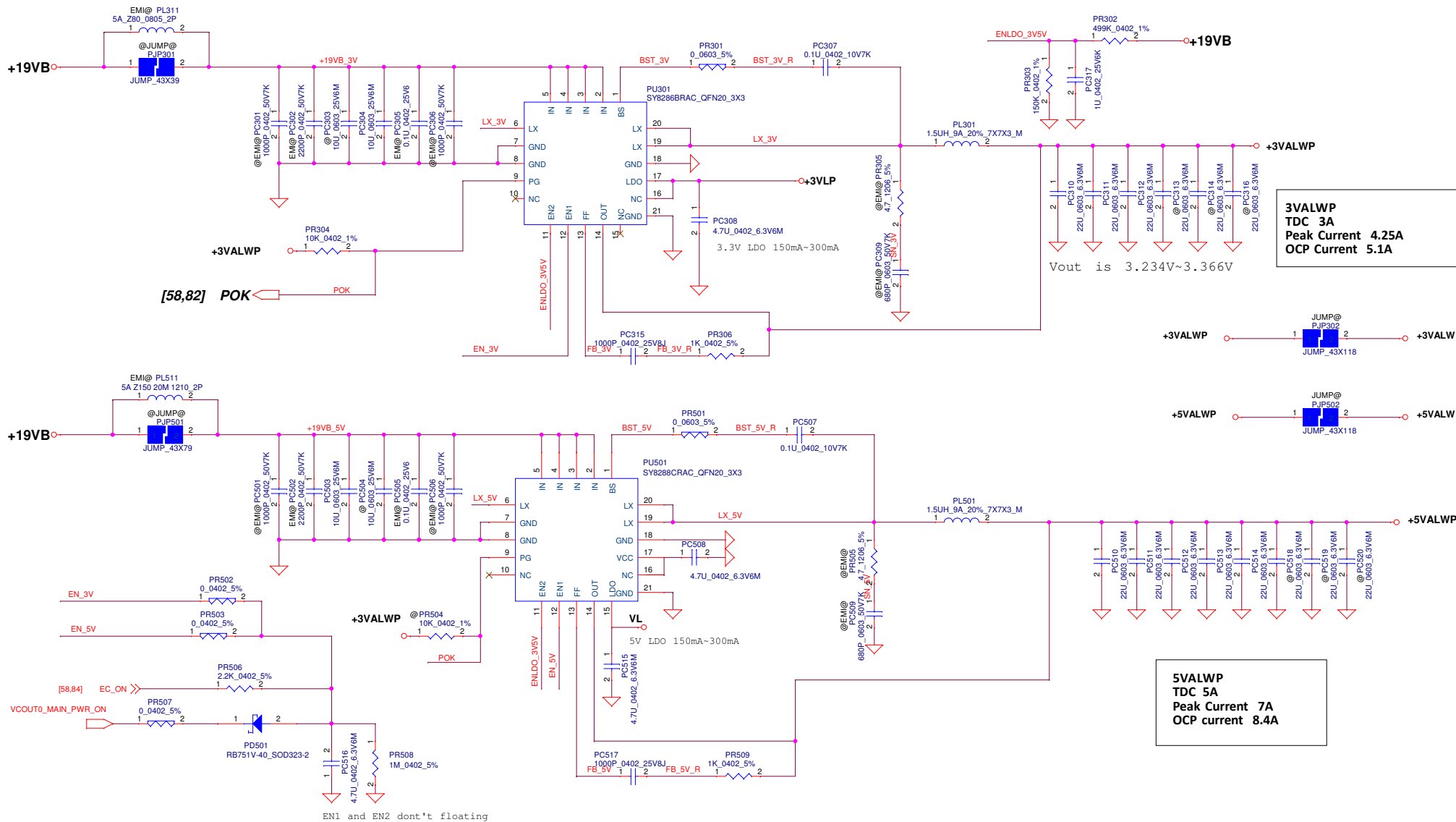
- PIN1 GND
- PIN2 GND
- PIN3 GND
- PIN4 SYS PRES
- PIN5 BATT PRS
- PIN6 DAT SMB
- PIN7 CLK SMB
- PIN8 Batt+
- PIN9 Batt+
- PIN10 Batt+
- SP021412220

ACES\_50458-01001-P01\_10P-T

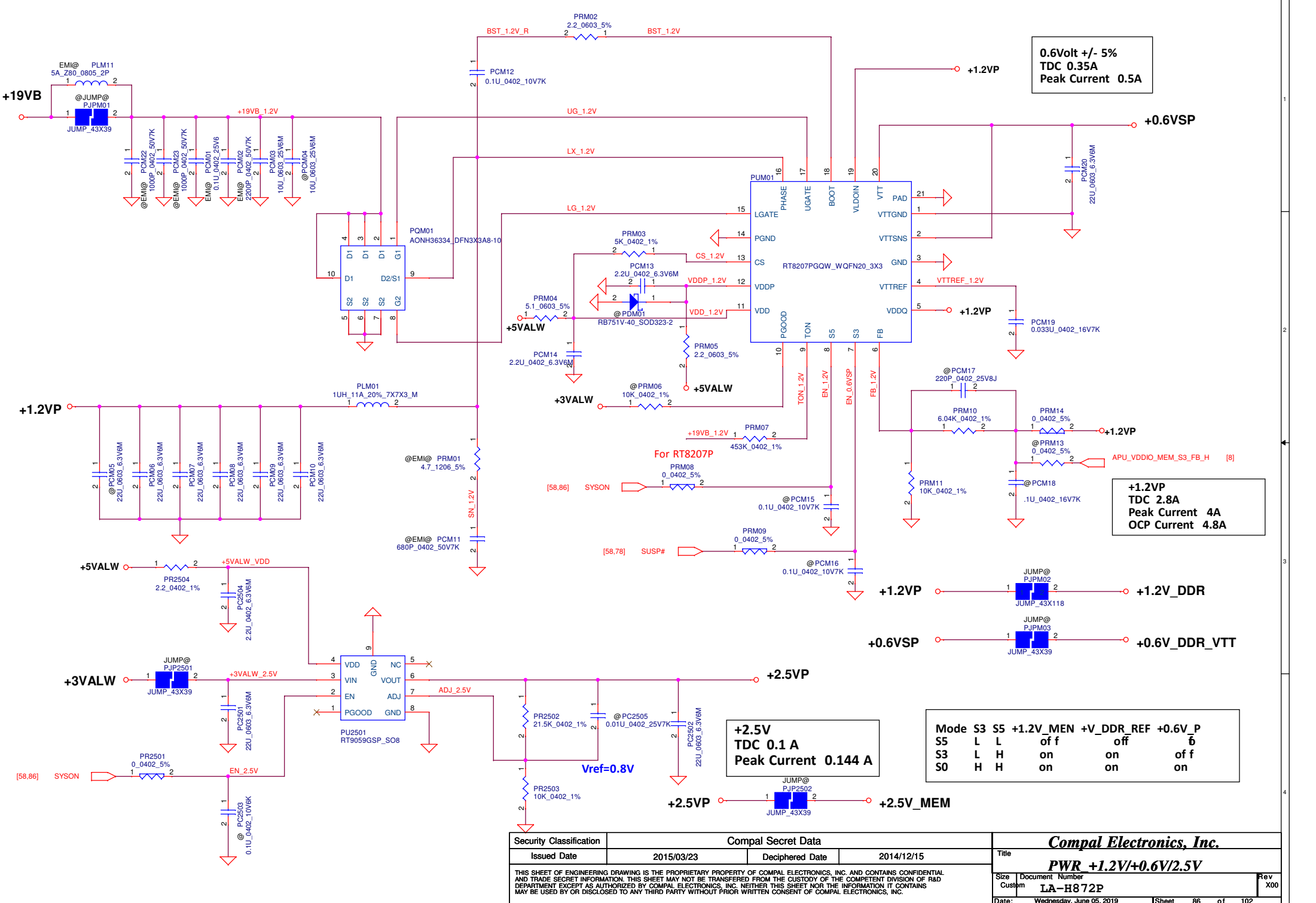


CPU thermal protection  
VCIN0\_PH  
Trig = 1V  
92 +/- 3 degree C  
Recover = 2.016V  
50 +/- 3 degree C





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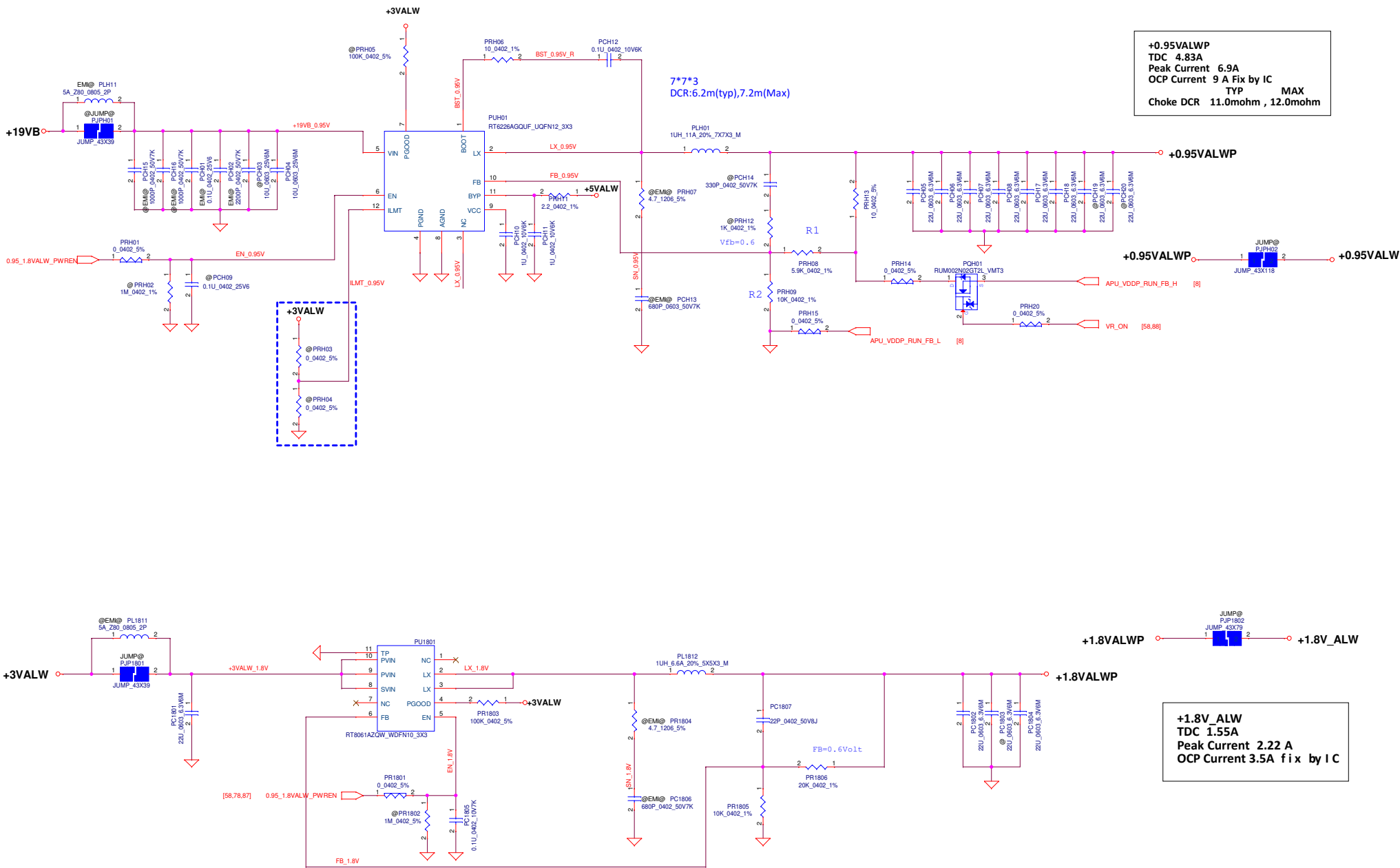
0.6Volt +/- 5%  
TDC 0.35A  
Peak Current 0.5A

+1.2VP  
TDC 2.8A  
Peak Current 4A  
OCP Current 4.8A

+2.5V  
TDC 0.1 A  
Peak Current 0.144 A

Mode	S3	S5	+1.2V_MEN	+V_DDR	REF	+0.6V_P
S5	L	L	of f	off	off	6
S3	L	H	on	on	of f	
S0	H	H	on	on	on	

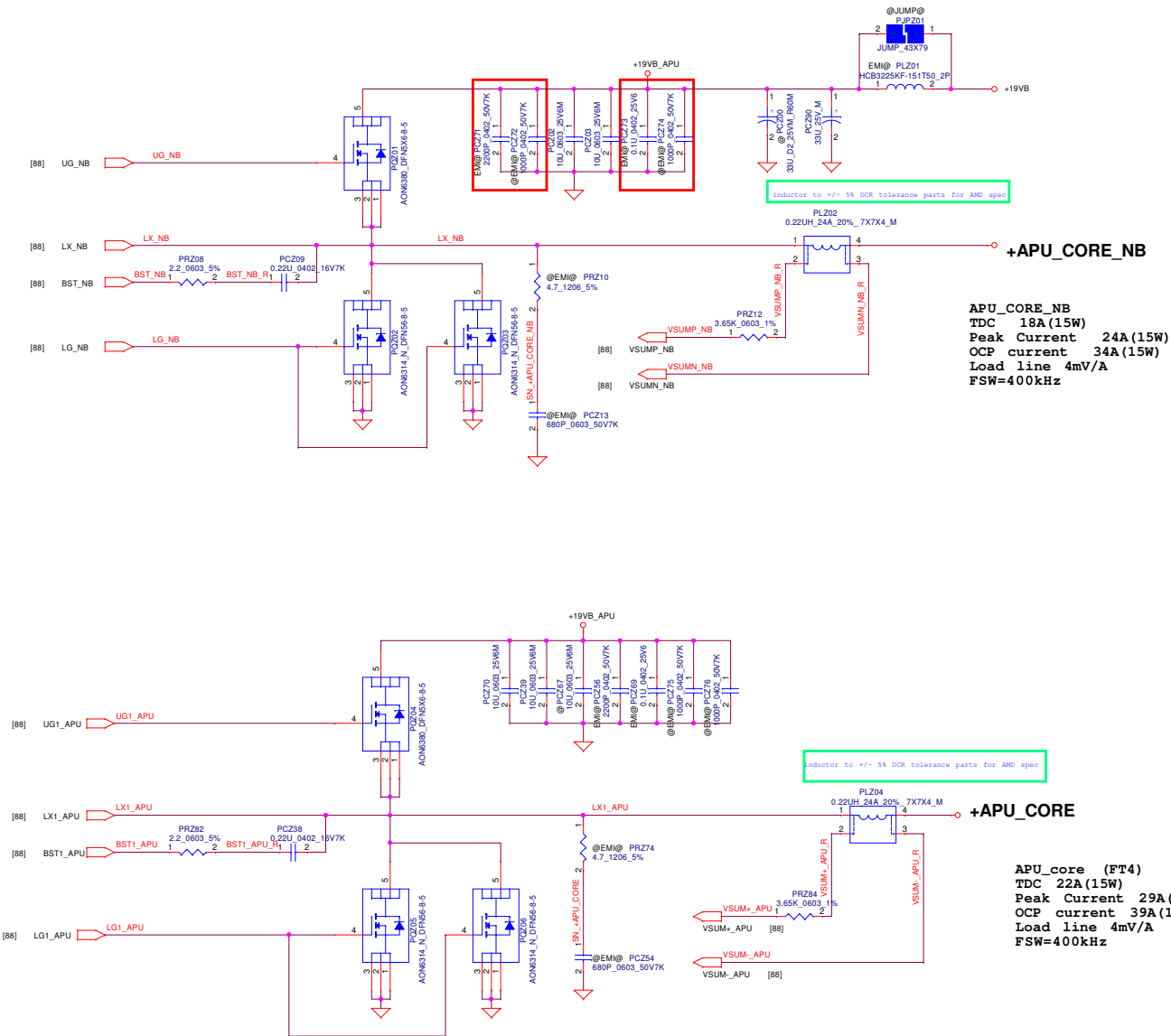
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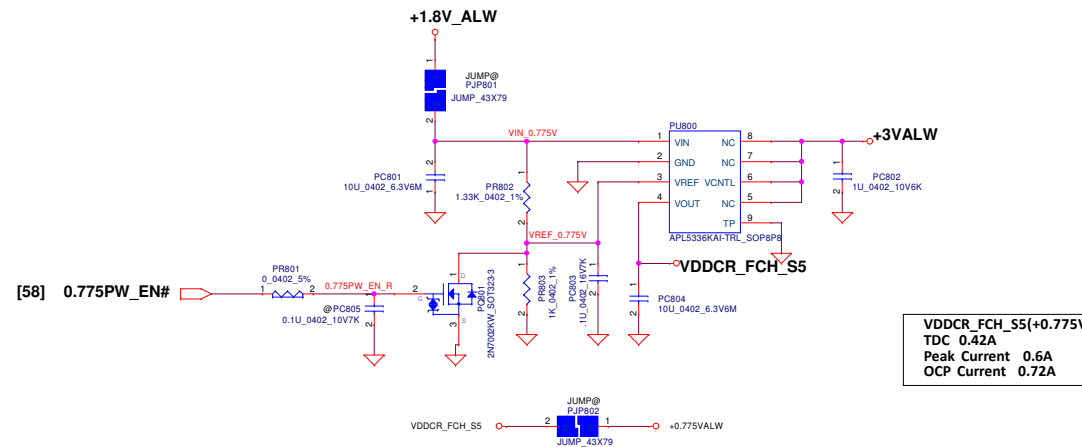


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The voltage level of 0.775PW\_EN must be low




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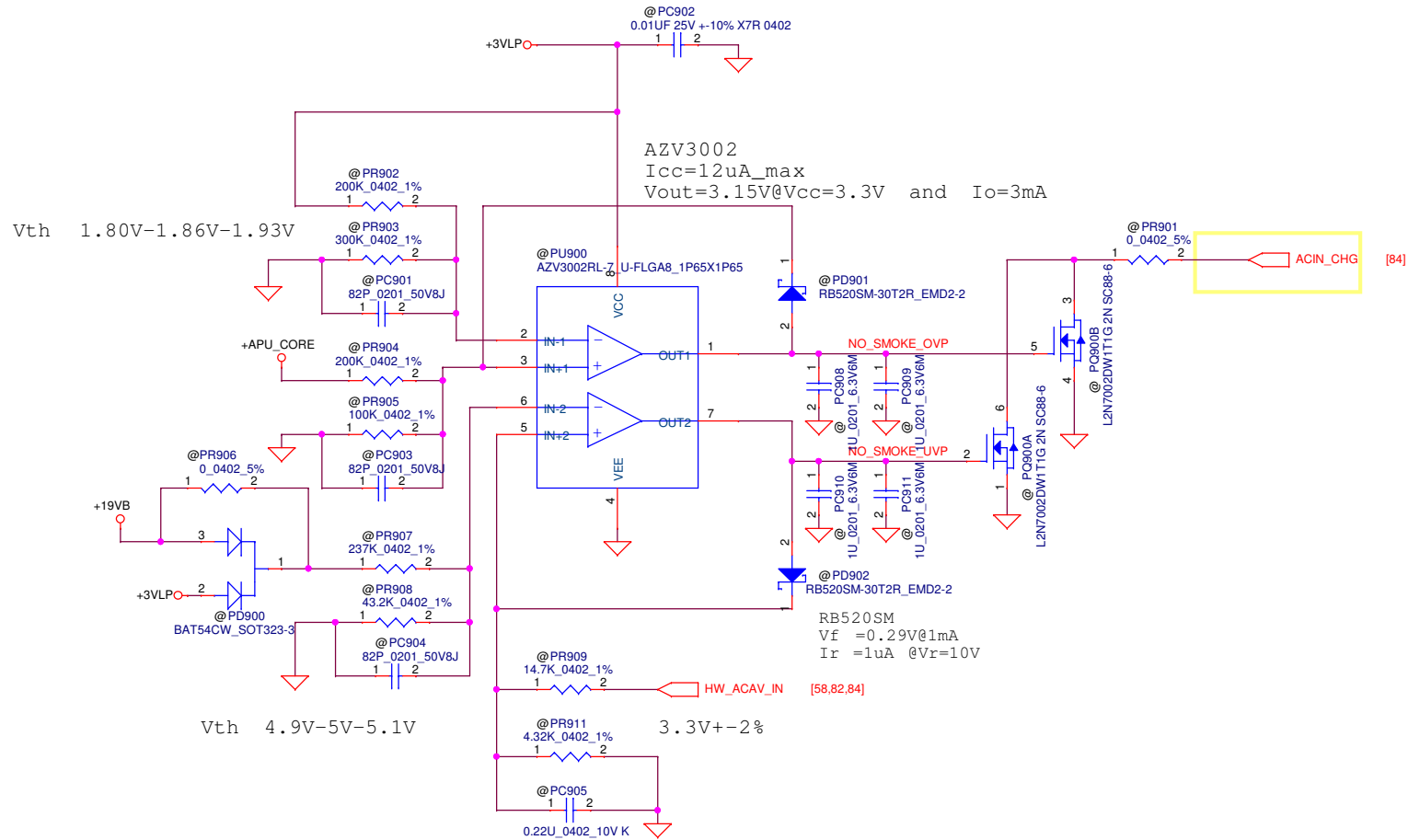
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BOM Change List:

GPIO Change List:

Design Change List:

# Pilot Change List :

BOM Change List:

GPIO Change List:

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